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PATENTS
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Eduard A. Cartier, et al.

Examiner: Lourdes C. Cruz

Serial No: 09/413,462

Art Unit: 2815

Filed: October 6, 1999

Docket: YOR919990358US1 (12906)

For: SILICATE GATE DIELECTRIC

Dated: March 15, 2002

Assistant Commissioner for Patents
United States Patent and Trademark Office
Washington, D.C. 20231

AMENDMENT AND RESPONSE

Sir:

In response to the Office Action dated December 21, 2001, applicants submit the following amendments and remarks for entry of record in the above-identified patent application.

IN THE SPECIFICATION:

Page 6, line 4, please add the following new paragraphs:

C1

--Fig. 10 is a pictorial representation (through a cross-sectional view) showing a field effect transistor (FET) of the present invention.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on March 15, 2002.

Dated: March 15, 2002

Mishelle Mustafa

Fig. 11 is a pictorial representation (through a cross-sectional view) showing a capacitor structure of the present invention.--

Page 11, line 27, please add the following new paragraphs:

Fig. 10 illustrates a cross-sectional view of a FET which includes the metal silicate described above as a dielectric material. Specifically, the FET shown in Fig. 10 includes Si-containing semiconductor substrate 11 having spaced apart source and drain regions 20 and 22, respectively defining channel 24 located therein. The FET also includes SiO_2 layer 16 located above channel 24, metal silicite layer 14 located atop SiO_2 layer 16, and gate electrode 26 located atop metal silicate layer 14. The gate electrode comprises polysilicon, W, Al or Pt.

Fig. 11 illustrates a cross-sectional view of a capacitor which include the metal silicate described above as a dielectric material. Specifically, the capacitor structure includes conductive electrodes 30 and 32 respectively, and SiO_2 layer 16 and metal silicate layer 14 sandwiched therebetween.--

IN THE CLAIMS:

Please cancel Claim 32 as well as non-elected Claims 1-20 and please amend Claims 21, 28 and 34 as follows:

~~21. (Twice Amended)~~ A semiconductor structure comprising at least one metal silicate dielectric material that is in direct contact ~~with a silicon~~ oxide layer, said silicon oxide layer being formed on a Si-containing substrate.

~~28. (Amended)~~ A field effect transistor comprising:

a Si-containing semiconductor ~~substrate~~;

spaced apart source/drain regions in said substrate defining ~~a channel~~ region therein;

Cl Cont Sub D2

a dielectric layer located atop said channel region, said dielectric layer including a bottom SiO_2 layer and a top ~~metal silicate~~ layer; and

a gate electrode formed over said top metal silicate layer.

Cl Sub D3

34. (Thrice Amended) A capacitor comprising a metal silicate dielectric material and a SiO_2 layer sandwiched ~~between~~ top and bottom electrode materials, wherein said at least one metal silicate is located directly atop said SiO_2 ~~layer.~~

REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, the drawings have been objected to under 37 C.F.R. §1.83(a) as allegedly not showing every feature recited in Claims 28-34. In response thereto, applicants have enclosed herewith a letter to the US Patent and Trademark Draftsman including a new sheet of drawings that show the features recited in Claims 28-34. Specifically, the new sheet of drawings includes Fig. 10 which shows a FET structure in accordance with Claims 28-33 and Fig. 11 which shows a capacitor structure in accordance with Claim 34. These new drawings will be incorporated into the formal drawings after the Examiner has approved the same.

In view of the above, applicants respectfully submit that the drawing objection has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

As a result of the above-proposed new drawings, applicants have amended the specification to include reference to the FET structure and the capacitor structure recited in the claims. This amendment was carried out to the text appearing at Page 11, line 27.

Support for the material added to Page 11, line 27 can be found in original Claims 28-34 as well as Page 4, lines 9-30 of the specification of the instant application.

Claim 34 stands rejected under 35 U.S.C. §112, second paragraph as allegedly indefinite since the term "the same" lacks antecedent basis in the claim. In response thereto, applicants have amended Claim 34 by deleting the phrase "the same or different" and the process limitations from the structure claim. Additionally, applicants have amended Claim 34 to positively recite that the claimed capacitor structure includes a metal silicate dielectric material and a SiO_2 layer sandwiched between top and bottom electrode materials, wherein the metal silicate is located directly atop the SiO_2 layer. Support for this amendment to Claim 34 is found in the processing steps of the present invention, see for example, Page 4, lines 13-16 of the specification of the instant application. Applicants respectfully submit that the above amendment to Claim 34 obviates the §112, second paragraph, rejection; therefore the instant rejection can and should be withdrawn.

Applicants have also amended Claim 21 to positively recite that the metal silicate is in direct contact with a SiO_2 layer. Support for this amendment to Claim 21 is found throughout the specification of the instant application. See, for example, Fig. 1b and Fig 2b. Additionally, applicants have amended Claim 28 by incorporating the subject matter of canceled Claim 32 therein. Non-elected Claims 1-20 have also been canceled in this amendment.

As required by 37 C.F.R. §1.121, applicants have attached a marked-up version of the changes made to the claims by the current amendment. The marked-up attachment is captioned "**VERSION WITH MARKINGS SHOWING CHANGES MADE**".

Claims 21-32 and 34 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent No. 5,313,089 to Jones, et al. ("Jones, et al."). Claim 33 stands rejected under 35 U.S.C. §103 as allegedly unpatentable over the combination of Jones, et al. and U.S. Patent No. 6,236,094 to Wright ("Wright").

It is axiomatic that anticipation under §102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986). Thus, there must be no differences between the subject matter of the claim and the disclosure of the applied prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: The absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants submit that Jones, et al. do not anticipate Claims 21-27 of the present application since the applied reference does not disclose a semiconductor structure comprising at least one metal silicate dielectric material that is in direct contact with a silicon oxide layer, said silicon oxide layer being formed on a Si-containing substrate. In contrast, Jones, et al. disclose in FIG 5 a capacitor comprising high-permitttivity dielectric region 36 which is sandwiched between conductive regions 38' and 38''. The high-permittivity material lies atop isolation or buffer layer 34 which is formed on dielectric material 30. Applicants find no disclosure in Jones, et al. of forming the high-permittivity material atop a SiO_2 layer which is formed atop a Si-containing substrate. Applicants submit that in FIG 10 Jones, et al. disclose a structure where high-permittivity layer 60 is formed over a transistor (not shown), a dielectric layer (not shown) or a substrate (not shown). Jones, et al. provide no teaching of

forming the high-permittivity material atop a SiO_2 layer which is formed atop a Si-containing substrate.

Insofar as Claims 28-31 and 33 are concerned, applicants respectfully submit that Jones, et al. do not disclose applicants' claimed FET which includes a Si-containing semiconductor substrate; spaced apart source/drain regions in said substrate defining a channel region therein; a dielectric layer located atop said channel region, said dielectric layer including a bottom SiO_2 layer and a top metal silicate layer; and a gate electrode formed over said top metal silicate layer. In contrast, the FET disclosed in Jones, et al. comprises substrate 12, source/drain regions 18 and 16, gate dielectric 24 and gate electrode 26. In accordance with Jones, et al. (See, Col. 3, lines 36-37) gate dielectric 24 is SiO_2. Applicants find no disclosure in Jones, et al. of a FET structure which includes a metallic silicate/SiO_2 stack as the gate dielectric material.

With regard to Claim 34, applicants respectfully submit that the claimed capacitor structure recited in Claim 34 is not anticipated by the disclosure of Jones, et al. since the applied reference does not disclose a capacitor comprising a metal silicate dielectric material and a SiO_2 layer sandwiched between top and bottom electrode materials, wherein said at least one metal silicate is located directly atop said SiO_2 layer. Instead, Jones, et al. disclose a capacitor structure comprising high-permitttivity dielectric region 36 which is sandwiched between vertical conductive regions 38' and 38''. The high-permittivity material lies atop isolation or buffer layer 34 which is formed on dielectric material 30. The prior art capacitor structure has vertical conductive regions, not top and bottom electrodes as presently claimed.

The foregoing remarks clearly indicate that the applied reference does not teach <u>each and every</u> aspect of the claimed invention, as required by <u>King</u> and <u>Kloster Speedsteel</u>;

therefore the claims of the present application are not anticipated by Jones, et al. Applicants thus respectfully submit that the instant §102(b) rejection has been obviated; therefore the anticipation rejection can and should be withdrawn.

Insofar as the §103 rejection to Claim 33 is concerned, applicants submit that the applied prior art references of Jones, et al. and Wright do not teach or suggest applicants' claimed FET structure which includes a Si-containing semiconductor substrate; spaced apart source/drain regions in said substrate defining a channel region therein; a dielectric layer located atop said channel region, said dielectric layer including a bottom SiO_2 layer and a top metal silicate layer; and a gate electrode formed over said top silicate layer. The primary reference spurring the §103 rejection, i.e., Jones, et al., is deficient for the same reasons as mentioned above concerning the §102(b) rejection; therefore those remarks are incorporated herein by reference. To reiterate: the FET disclosed in Jones, et al. comprises substrate 12, source/drain regions 18 and 16, gate dielectric 24 and gate electrode 26. In accordance with Jones, et al. (See, Col. 3, lines 36-37) gate dielectric 24 is SiO_2. Applicants find no disclosure in Jones, et al. of a FET structure which includes a metallic silicate/SiO_2 stack as the gate dielectric material.

The above defect in Jones, et al. is not alleviated by Wright since the applied reference does not teach or suggest applicants' claimed FET which includes a gate dielectric layer that comprises a bottom SiO_2 layer and a metal silicate formed thereon. In contrast, the FET structure disclosed in Wright comprises substrate 302 having source and drain regions 310 and 312 formed therein which define channel region 305. The prior art FET includes gate dielectric 306 such as SiO_2 formed above the channel, gate electrode 308 formed atop of the gate dielectric and low resistance metal such as Al or W formed atop the gate electrode.

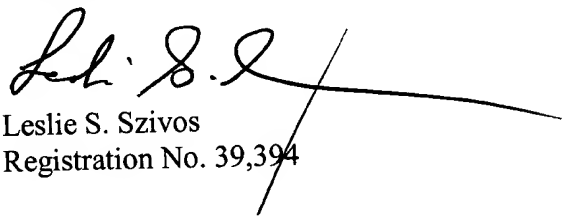
Applicants respectfully submit the Wright does not teach or suggest the claimed dielectric stack as the gate dielectric for a FET.

The §103 rejection also fails because there is no motivation in the applied references which suggest modifying the FET structures disclosed in either applied prior art reference to arrive at applicants' claimed FET structure which includes a gate dielectric which includes a bottom SiO_2 layer and a top metal silicate layer. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejection under 35 U.S.C. §103 has been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,



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